EXPRESS EV 425039[redacted]05US

PATENT COOPERATION TREATY

PCT/PTO 25 OCT 2004 10/51[redacted]7

From the
INTERNATIONAL PRELIMINARY EXAMINING AUTHORITY

To:
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Dothe 350

PCT

NOTIFICATION OF TRANSMITTAL OF INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Rule 71.1)

Date of Mailing *(day/month/year)*	30 AUG 2004

Applicant's or agent's file reference	**IMPORTANT NOTIFICATION**
PU020119	

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US03/11207	10 April 2003 (10.04.2003)	17 April 2002 (17.04.2002)

Applicant

THOMSON LICENSING S.A.

1. The applicant is hereby notified that this International Preliminary Examining Authority transmits herewith the international preliminary examination report and its annexes, if any, established on the international application.

2. A copy of the report and its annexes, if any, is being transmitted to the International Bureau for communication to all the elected Offices.

3. Where required by any of the elected Offices, the International Bureau will prepare an English translation of the report (but not of any annexes) and will transmit such translation to those Offices.

4. **REMINDER**

The applicant must enter the national phase before each elected Office by performing certain acts (filing translations and paying national fees) within 30 months from the priority date (or later in some Offices)(Article 39(1))(see also the reminder sent by the International Bureau with Form PCT/IB/301).

Where a translation of the international application must be furnished to an elected Office, that translation must contain a translation of any annexes to the international preliminary examination report. It is the applicant's responsibility to prepare and furnish such translation directly to each elected Office concerned.

For further details on the applicable time limits and requirements of the elected Offices, see Volume II of the PCT Applicant's Guide.

Name and mailing address of the IPEA/US	Authorized officer
Mail Stop PCT, Attn: IPEA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450	Emmanuel Bayard
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Form PCT/IPEA/416 (July 1992)

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

(PCT Article 36 and Rule 70)

Applicant' s or agent' s file reference PU020119	**FOR FURTHER ACTION**	See Notification of Transmittal of International Preliminary Examination Report (Form PCT/IPEA/416)
International application No, PCT/US03/11207	International filing date *(day/month/year)* 10 April 2003 (10.04.2003)	Priority date *(day/month/year)* 17 April 2002 (17.04.2002)
International Patent Classification (IPC) or national classification and IPC IPC(7): H03H 7/30; H03K 5/159 and US Cl.: 375/232, 233		
Applicant THOMSON LICENSING S.A.		

1. This international preliminary examination report has been prepared by this International Preliminary Examining Authority and is transmitted to the applicant according to Article 36.

2. This REPORT consists of a total of 5 sheets, including this cover sheet.

☐ This report is also accompanied by ANNEXES, i.e., sheets of the description, claims and/or drawings which have been amended and are the basis for this report and/or sheets containing rectifications made before this Authority (see Rule 70.16 and Section 607 of the Administrative Instructions under the PCT).

These annexes consist of a total of ___ sheets.

3. This report contains indications relating to the following items:

- I ☒ Basis of the report
- II ☐ Priority
- III ☐ Non-establishment of report with regard to novelty, inventive step and industrial applicability
- IV ☐ Lack of unity of invention
- V ☒ Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- VI ☐ Certain documents cited
- VII ☐ Certain defects in the international application
- VIII ☐ Certain observations on the international application

Date of submission of the demand	Date of completion of this report
17 November 2003 (17.11.2003)	21 August 2004 (21.08.2004)
Name and mailing address of the IPEA/US Mail Stop PCT, Attn: IPEA/US Commissioner for Patents P.O. Box 1450 Alexandria, Virginia 22313-1450 Facsimile No. (703) 305-3230	Authorized officer Emmanuel Bayard Telephone No. 703-308-9573

Form PCT/IPEA/409 (cover sheet)(July 1998)

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US03/11207

I. Basis of the report

1. With regard to the elements of the international application:*

☒ the international application as originally filed.

☒ the description:
pages 1-17 as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

☒ the claims:
pages 18-25, as originally filed
pages NONE, as amended (together with any statement) under Article 19
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

☒ the drawings:
pages 1-4, as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

☐ the sequence listing part of the description:
pages NONE, as originally filed
pages NONE, filed with the demand
pages NONE, filed with the letter of _____.

2. With regard to the **language**, all the elements marked above were available or furnished to this Authority in the language in which the international application was filed, unless otherwise indicated under this item.
These elements were available or furnished to this Authority in the following language _____ which is:

☐ the language of a translation furnished for the purposes of international search (under Rule23.1(b)).

☐ the language of publication of the international application (under Rule 48.3(b)).

☐ the language of the translation furnished for the purposes of international preliminary examination(under Rules 55.2 and/or 55.3).

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, the international preliminary examination was carried out on the basis of the sequence listing:

☐ contained in the international application in printed form.

☐ filed together with the international application in computer readable form.

☐ furnished subsequently to this Authority in written form.

☐ furnished subsequently to this Authority in computer readable form.

☐ The statement that the subsequently furnished written sequence listing does not go beyond the disclosure in the international application as filed has been furnished.

☐ The statement that the information recorded in computer readable form is identical to the written sequence listing has been furnished.

4. ☒ The amendments have resulted in the cancellation of:

☒ the description, pages NONE

☒ the claims, Nos. NONE

☒ the drawings, sheets/~~fig~~ NONE

5. ☐ This report has been established as if (some of) the amendments had not been made, since they have been considered to go beyond the disclosure as filed, as indicated in the Supplemental Box (Rule 70.2(c)).**

** Replacement sheets which have been furnished to the receiving Office in response to an invitation under Article 14 are referred to in this report as "originally filed" and are not annexed to this report since they do not contain amendments (Rules 70.16 and 70.17).*

*** Any replacement sheet containing such amendments must be referred to under item 1 and annexed to this report.*

INTERNATIONAL PRELIMINARY EXAMINATION REPORT

International application No.
PCT/US03/11207

V. Reasoned statement under Rule 66.2(a)(ii) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement

1. STATEMENT

Novelty (N)	Claims NONE	YES
	Claims 1-25	NO
Inventive Step (IS)	Claims NONE	YES
	Claims 1-25	NO
Industrial Applicability (IA)	Claims 1-25	YES
	Claims NONE	NO

2. CITATIONS AND EXPLANATIONS
Please See Continuation Sheet

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

Claims 1-25 lack novelty under PCT Article 33(2) as being anticipated by Ishikawa et al U.S. patent No 5,455,844.

As per claims 1 and 16, Ishikawa teaches a mode selector apparatus (FIG. 7) for automatically selecting one of a standard automatic switching mode and a soft automatic switching mode in a decision feedback equalizer (DFE), said mode selector apparatus being adapted for use in a data signal processing system with equalization, said mode selector apparatus comprising:

an equalizer (30) for providing first and second DFE outputs corresponding to a standard dd mode and a soft dd mode, respectively (see fig.1 and abstract and col.5, lines 15-46); and a comparator (36) for comparing (see fig.1 element 31 and col.5, lines 28-35) byte error rates (ByER) of said first and second DFE outputs for selecting as a superior mode that mode associated with a lower ByER and outputting the DFE output with said lower ByER.

As per claim 2, Ishikawa inherently includes said standard automatic switching mode selectively exhibiting a blind mode and a standard decision directed (dd) mode and said soft automatic switching mode selectively exhibiting a blind mode and a soft dd mode.

As per claim 3, Ishikawa inherently includes said lock detector means (30) for providing a lock signal for indicating convergence of said DFE, said lock signal being derived from said DFE output signal with said lower BER.

As per claim 4, Ishikawa inherently includes said equalizer (30) for providing said first and second DFE output signals comprises decision feedback equalizer (DFE) means for processing said data signal and exhibiting concurrent soft and hard decision directed (dd) output signals.

As per claim 5, Ishikawa inherently includes said lock detector means (30) includes first and second lock detectors (30) for providing respective lock signals derived from respective ones of said DFE outputs.

As per claim 6, Ishikawa inherently includes a mode switch (38) for selectively placing said DFE outputs in one of (a) one of said standard and soft dd modes and (b) a blind mode, depending on said lock signal identifying convergence of said DFE.

As per claim 7, Ishikawa inherently includes said a training mode replaces the blind mode and including a mode switch (38) for selectively placing said DFE outputs in one of (a) ore of said standard and soft dd modes and (b) a training mode, depending on said lock signal identifying convergence of said DFE.

As per claim 8, Ishikawa inherently includes a forward error correcting processor (32, 34) for processing said first and second DFE output signals by forward error correction (FEC) so as to provide respective first and second FEC output signals; wherein: the comparator (36) determines which one of said standard automatic
switching mode and said soft automatic switching mode is the superior mole ire accordance with a defined comparison criterion, and outputs an output signal of said one superior mode.

As per claim 9, Ishikawa inherently includes said forward error correcting processor (32, 34) includes a trellis decoder (32, 34) and a Reed Solomon (RS) decoder (32, 34).

As per claim 10, Ishikawa inherently includes said detined comparison criterion comprises said comparator (36) comparing

Supplemental Box
(To be used when the space in any of the preceding boxes is not sufficient)

uncorrectable segment rates (USR) out of said RS decoder, selecting as a superior mode that mode associated with a lower USR and outputting the DFE output signal with said lower USR.

As per claim 11, Ishikawa inherently includes said defined comparison criterion comprises said comparator (36) comparing estimated bit error rate (BER) out of said RS decoder, selecting as a superior mode that mode associated with a lower BER and outputting the DFE output signal with said lower BER.

As per claim 12, Ishikawa inherently includes said equalizer for providing first and second DFE output signals includes equalizer filtering means and slicer means (30) coupled to said mode switch (38) for providing said first and second DFE output signals.

As per claim 13, Ishikawa inherently includes said forward error correcting processor comprises parallel processing means (32, 34) for respectively providing said first and second FEC output signals.

As per claim 14, Ishikawa inherently includes a mode switch coupled to said first and second DFE output signals, said respective lock output signals, and to said comparison signal for monitoring said comparison signal for selecting one of said respective lock output signals to provide said lock signal, depending upon said comparison signal.

As per claim 15, Ishikawa inherently includes said mode switch (38) selects one of said respective lock output signals corresponding to said superior mode.

As per claim 17, Ishikawa inherently includes said step of utilizing said selection signal for controlling said DFE comprises a step of setting said DFE into one of (a) a blind mode, and (b) one of a standard decision directed mode and a soft decision directed mode, depending on said selection signal.

As per claim 18, Ishikawa inherently includes said step for providing first and second DFE output signals includes: a step of equalizer filtering; and a step of signal slicing coupled for providing said first and second DFE output signals.

As per claim 19, Ishikawa inherently includes said step of processing said first and second DFE output signals comprises a step of processing said first and second DFE output signals in parallel paths for respectively providing said first and second FEC output signals.

As per claim 21, Ishikawa inherently includes said step of FEC processing includes steps of trellis decoding and Reed Solomon decoding.

As per claim 21, Ishikawa inherently includes said step of utilizing said selection signal for controlling said DFE comprises: deriving a first lock signal from said first FEC output signal; deriving a second lock signal from said second FEC output signal; and selecting one of said first anti second lock signals for controlling said DFE, depending on said selection signal.

As per claim 22, Ishikawa inherently includes said step of processing said first and second DFE output signals comprises a step of processing said data signal by a decision feedback equalizer (DFE) exhibiting concurrent soft and hard decision directed (dd) operating modes for providing said first and second DFE output signals.

As per claim 23, Ishikawa inherently includes providing concurrently in each output symbol soft decision bit representation concurrently both hard and soft decision representations.

As per claim 24, Ishikawa inherently includes said step of utilizing said selection signal for controlling said DFE comprises: deriving a lock signal from one of said first and second FEC output signal, depending on said selection signal; and utilizing said lock signal for controlling said DFE.

As per claim 25, Ishikawa inherently includes said step of Utilizing said selection signal for controlling said DFh comprises: deriving said lock signal from that one of said first arid second FEC output signal associated with said superior mode.